偉詮電子股份有限公司
Weltrend Semiconductor, Inc.

WT5700
Capacitive Touch Key Sensor

Data Sheet

Rev. 1.00

July 10, 2009

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Update package information

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Update package information

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Add SSOP24 package
Modify Block Diagram

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Update package information

V0.91 9/23/2008
Add description

V0.90 9/9/2008
Preliminary data sheet.

Table of Contents

1 General Description

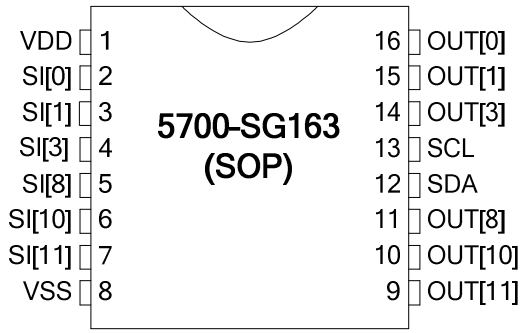
WT5700 is a 1-12 keys capacitive touch key sensor. It is designed for replacing button and also can be configured as matrix scan function. WT5700 has low power consumption, so it is suitable for consumer products and portable applications.

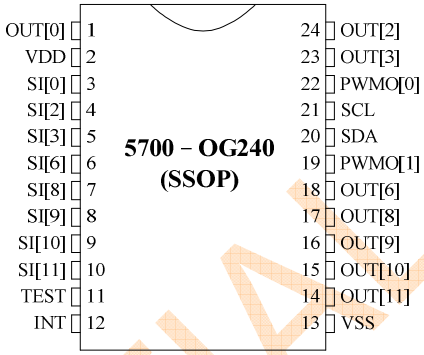
1.1. Features

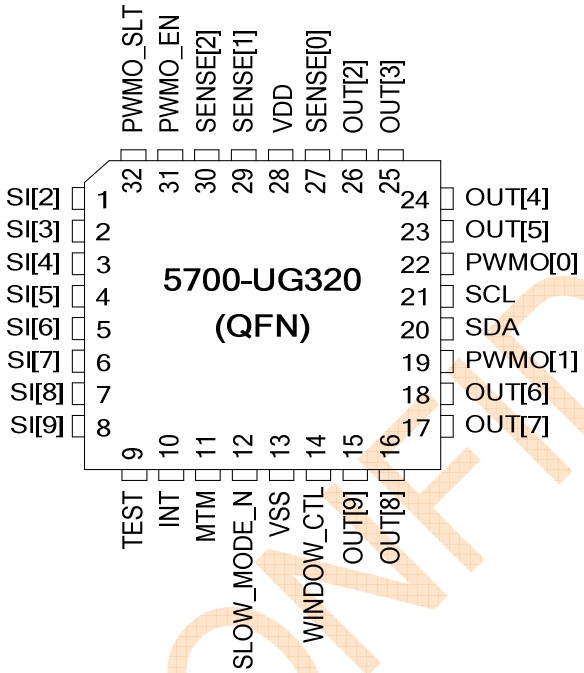
- 1-12 channel input sensor
- Auto sensitivity calibration
- 3 sensitivity option pins
- 2 sensitivity control registers
- Anti-noise circuit embedded
- 24ms response time
- 3 output modes
  - Direct output: 12 output pad (open drain output)
  - Serial output(I2C) and include interrupt pin
  - PWM output
- Output polarity option: active high or active low
- 6 output expander(maximum)
- Open-drain digital output with maximum drain current 8mA
- Wild operating voltage: 2.2V ~ 5.5V
- 3 operation modes: Normal mode, Slow down mode and Sleep mode
- Low operating current
  - Normal mode
    - 3.3V: Typical 150uA
    - 5.0V: Typical 315uA
  - Slow down mode
    - 3.3V: Typical 35uA
    - 5.0V: Typical 75uA
  - Sleep mode
    - 3.3V: Typical 0.6uA
    - 5.0V: Typical 0.7uA
- Package type
  - LQFP48
  - QFN32
  - SSOP24
  - SOP16

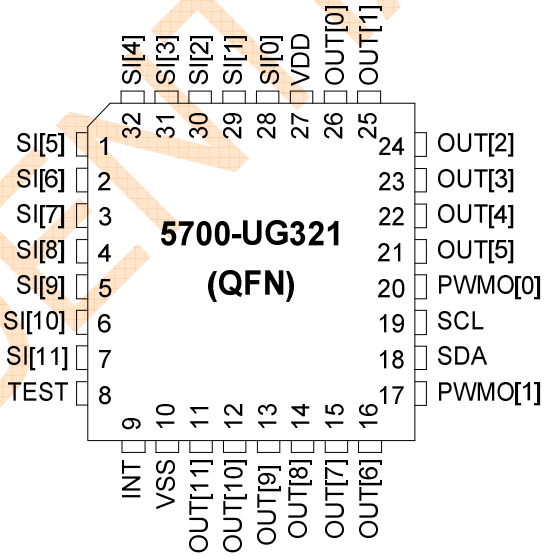
2. Pin Assignment

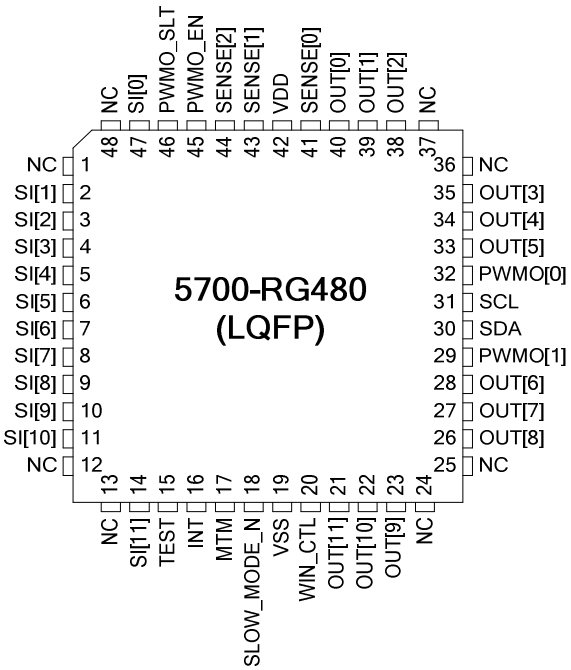
2.1. Package











2.2. Ordering information

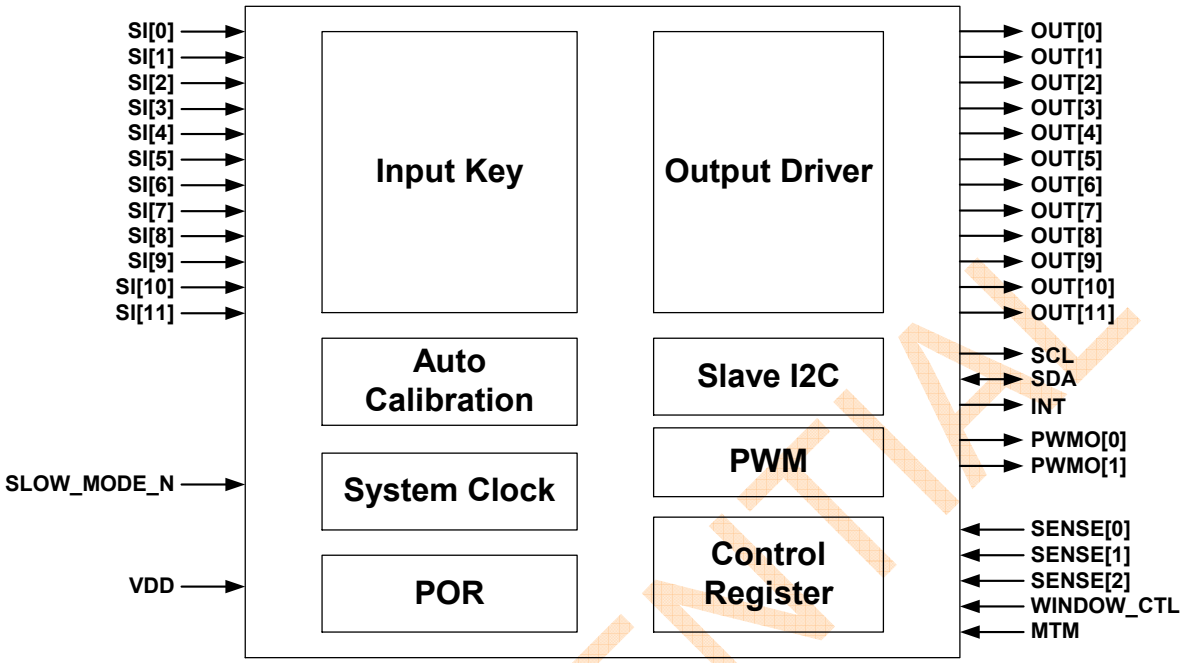
Package Type	Package Outline	Part Number
SOP 16 pin	150mil	5700-SG163WT
SSOP 24 pin	150mil	5700-OG240WT
QFN 32 pin	5mm * 5 mm	5700-UG320WT
QFN 32 pin	5mm * 5 mm	5700-UG321WT
LQFP 48 pin	7mm * 7 mm	5700-RG480WT

2.3. Pin description

R480	U320	U321	O240	S163	Pin Name	I/O	Function Description
47		28	3	2	SI[0]	A	Capacitive sensor input[0]
2		29		3	SI[1]	A	Capacitive sensor input[1]
3	1	30	4		SI[2]	A	Capacitive sensor input[2]
4	2	31	5	4	SI[3]	A	Capacitive sensor input[3]
5	3	32			SI[4]	A	Capacitive sensor input[4]
6	4	1			SI[5]	A	Capacitive sensor input[5]
7	5	2	6		SI[6]	A	Capacitive sensor input[6]
8	6	3			SI[7]	A	Capacitive sensor input[7]
9	7	4	7	5	SI[8]	A	Capacitive sensor input[8]
10	8	5	8		SI[9]	A	Capacitive sensor input[9]
11		6	9	6	SI[10]	A	Capacitive sensor input[10]
14		7	10	7	SI[11]	A	Capacitive sensor input[11]
15	9	8	11		TEST	I	Test mode pin (internal pull high)
16	10	9	12		INT	O	Interruption output
17	11				MTM	I	Multi touch mode select input (internal pull high)
18	12				SLOW_MODE_N	I	RC oscillator frequency slow down mode (internal pull high)
19	13	10	13	8	VSS	P	ground
20	14				WIN_CTL	I	Window sensitivity control (internal pull high)
21		11	14	9	OUT[11]	O	Channel of output[11] (Open drain)
22		12	15	10	OUT[10]	O	Channel of output[10] (Open drain)
23	15	13	16		OUT[9]	O	Channel of output[9] (Open drain)
26	16	14	17	11	OUT[8]	O	Channel of output[8] (Open drain)
27	17	15			OUT[7]	O	Channel of output[7] (Open drain)
28	18	16	18		OUT[6]	O	Channel of output[6] (Open drain)
29	19	17	19		PWMO[1]	O	PWMO[1] output
30	20	18	20	12	SDA	I/O	I2C SDA
31	21	19	21	13	SCL	I	I2C SCL
32	22	20	22		PWMO[[0]	O	PWMO[[0] output
33	23	21			OUT[5]	O	Channel of output[5] (Open drain)
34	24	22			OUT[4]	O	Channel of output[4] (Open drain)
35	25	23	23	14	OUT[3]	O	Channel of output[3] (Open drain)
38	26	24	24		OUT[2]	O	Channel of output[2] (Open drain)
39		25		15	OUT[1]	O	Channel of output[1] (Open drain)
40		26	1	16	OUT[0]	O	Channel of output[0] (Open drain)
41	27				SENSE[0]	I	Sensitivity control [0] (internal pull high)
42	28	27	2	1	VDD	P	VDD
43	29				SENSE[1]	I	Sensitivity control [1] (internal pull high)
44	30				SENSE[2]	I	Sensitivity control [2] (internal pull high)
45	31				PWMO_EN	I	PWMO output enable (internal pull high)
46	32				PWMO_SLT	I	PWMO output mode selection (internal pull high)

A: analog, O: output, I: input, P: power

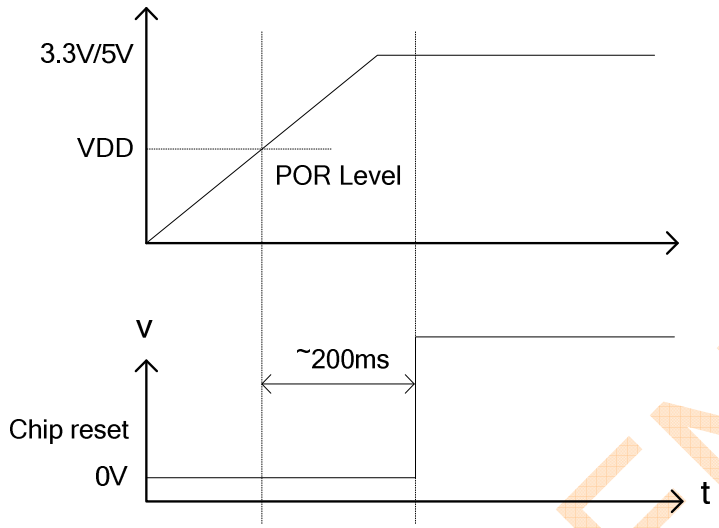
3. Functional Block Diagram



4. Functional Description

4.1. Chip initialization

After VDD rises over POR(power on reset), the internal reset signal will be kept active about 200ms(@VDD=3.3V) and then be released



4.2. System control register

Index	Default	R/W	Bit	Name	Description
00	60	R/W	7	Reserved	
		R/W	6	HEAVY_LOAD_N	Faster sample clock for heavy load. 1: Disable 0: Enable
		R/W	5	SLOW_MODE_N	System and sample oscillator slow down mode for power saving. 1: Normal mode 0: Slow down mode
		W	4	RST_CALB	1: Reset calibration block and new calibration starts 0: normal mode
		R/W	3	ACT_INT_LVL	Interruption active level 1: High active 0: Low active
		R/W	2	ACT_OUT_LVL	Detect output active level 1: High active 0: Low active
		R/W	1	CTL_SLT	Control signal selection 1: From register setting (controlled by IIC) 0: From input pin (controlled by pin)
		R/W	0	PWR_DN	1: Power down oscillator 0: Normal mode

(a) If MUC sends I2C command to set CTL_SLT=1, the function of control input pin will be disable. The control signals include SENSE[2:0], WIN_CTL, MTM, PWMO_EN, PWMO_SLT, SLOW_MODE_N, and HEAVY_LOAD_N.
(b) PWR_DN: MCU sends I2C command to enable/disable power down mode(sleep mode).
(c) After wake up, MCU must set RST_CALB=1 to reset calibration block and get new & correct calibration data.

4.3. I2C interface

If MUC sends command to set CTL_SLT=1(index:00H,bit1), the function of control input pin will be disable. Control signals include: SENSE[2:0], WIN_CTL, MTM, PWMO_EN, PWMO_SLT, SLOW_MODE_N, HEAVY_LOAD_N.

4.3.1. Slave I2C Command format

(A) Slave I2C write mode:
Start + saddr(E0) + A + 00 + A + addr + A + data1 + A+ - - - + dataN + A + Stop

(B) Slave I2C read mode:
Start + saddr(E0) + A + 00 + A + addr + Stop +
Start + saddr(E1) + A + data1 + A + - - - + dataN + NACK + Stop

4.4. Pin and Register control signal

4.4.1. Control register

Index	Default	R/W	Bit	Name	Description
02	F7	R/W	7	PWMO_EN	Enable PWM output
			6	PWMO_SLT	PWM output mode selection 1: PWM[0] output SI[0]/SI[2]/SI[4]/SI[6]/SI[8]/SI[10] PWM[1] output SI[1]/SI[3]/SI[5]/SI[7]/SI[9]/SI[11] 0: PWM[0] output SI[0]/SI[1]……./SI[10]/SI[11]
			5	MTM	Default =1 1: Multi touch mode 0: Single touch mode
			4	WIN_CTL	Window sensitivity control 1: No-windows sensitivity 0:1/2-windows sensitivity
			3	Reserved	
			2-0	SENSE1[2:0]	Sensitivity level selection for group 1 (SI[11:7], SI[5:1]) 000: 4 clock 001: 8 clock 010: 12 clock 011: 20 clock 100: 32 clock 101: 48 clock 110: 72 clock 111: 96 clock
03	07	R/W	7-3	Reserved	
			2-0	SENSE2[2:0]	Sensitivity level selection for group 2 (SI[6], SI[0]) 000: 4 clock 001: 8 clock 010: 12 clock 011: 20 clock 100: 32 clock 101: 48 clock 110: 72 clock 111: 96 clock

(a) Initial “are same as status of “INPUT” pin.
“CONTROL” data includes SENSE[2:0], WIN_CTL, MTM, PWMO_EN, PWMO_SLT, SLOW_MODE_N, HEAVY_LOAD_N.

(b) SI sensitivity source from pin or register

	CTL_SLT =0	CTL_SLT=1
SI[11:7], SI[5:1]	SENSE[2:0] pins	SENSE1[2:0] register
SI[6], SI[0]	SENSE[2:0] pins	SENSE2[2:0] register

(c) MTM=0 : single touch mode. The lower number input has more prior output. SI[0] is the most prior output and SI[11] is the most posterior

4.4.2. Sensitivity and Window control: SENSE[2:0] & WIN_CTL

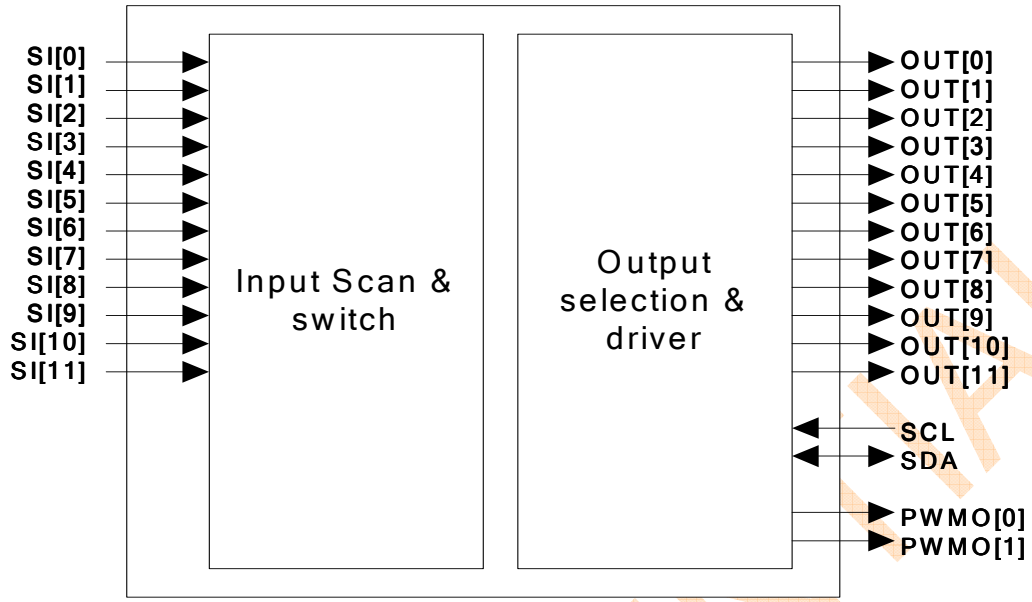
(A) The key detector is the value (different clock numbers) of clock difference for detecting from no-touching to touching.

SENSE[2:0]			Clock difference
0	0	0	4
0	0	1	8
0	1	0	12
0	1	1	20
1	0	0	32
1	0	1	48
1	1	0	72
1	1	1	96

(B) The key from touching to release detect by WIN_CTL.

SENSE [2:0]			WIN_CTL	
			1 No-W	0 1/2-W
0	0	0	4	2
0	0	1	8	4
0	1	0	12	6
0	1	1	20	10
1	0	0	32	16
1	0	1	48	24
1	1	0	72	36
1	1	1	96	48

4.5. Output interface



4.5.1. Direct output : OUT[11:0]

Direct mode : IN pad (SI[0]-SI[11]) => output pad(OUT[0]-OUT[11]))
(1) Multi touch mode(MTM=1, (index:20H,bit5))
(2) Single touch mode(MTM=0, (index:20H,bit5))

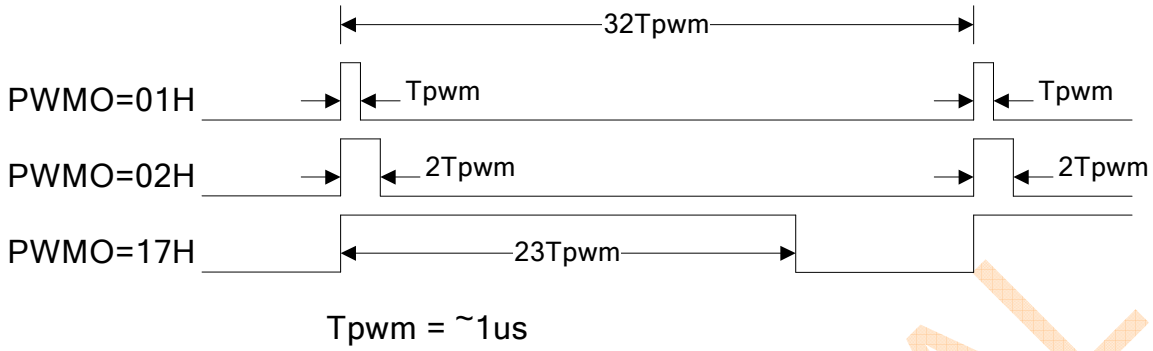
4.5.2. PWMO output: PWMO[1:0]

(1) PWMO_SLT register :
(a) PWMO_SLT=1 : PWMO[0] outputs the dectection of SI[0]/SI[2]/SI[4]/SI[6]/SI[8]/SI[10]
PWMO[1] outputs the dectection of SI[1]/SI[3]/SI[5]/SI[7]/SI[9]/SI[11]
(b) PWMO_SLT=0 : PWMO[0] outputs the dectection of SI[0]/SI[1]...../SI[10]/SI[11]
PWMO[1] is no use.

Touched PAD	PWMO_SLT=0	PWMO_SLT=1	
	PWMO[0] output	PWMO[0] output	PWMO[1] output
SI[0]	01H	02H	
SI[1]	03H		02H
SI[2]	05H	06H	
SI[3]	07H		06H
SI[4]	09H	0AH	
SI[5]	0BH		0AH
SI[6]	0DH	0EH	
SI[7]	0FH		0EH
SI[8]	11H	12H	
SI[9]	13H		12H
SI[10]	15H	16H	
SI[11]	17H		16H

(2) PWMO base clock ~= 1Mhz, => PWMO period = 1Mhz/32=31.25kH

(3) PWMO-outputs only support single-touch mode



4.5.3. I2C serial interface

(1) Sensor data(KEY_TOUCH[11:0]) always supports multi-touch mode.

Index	Default	R/W	Bit	Name	Description
08	00	R	7-4	Reserved	
			3-0	KEY_TOUCH [11:8]	0000: No key of SI[11:8] has been touched 0001: SI[8] key has been touched 0010: SI[9] key has been touched 0011: SI[9:8] keys have been touched | 1111: SI[11:8] keys have been touched
09	00	R	7-0	KEY_TOUCH [7:0]	0000_0000: No key of SI[7:0] has been touched 0000_0001: SI[0] key has been touched 0000_0010: SI[1] key has been touched 0000_0011: SI[1:0] keys have been touched | 1111_1111: SI[7:0] keys have been touched

(2) SI[11:0] Sample counter.

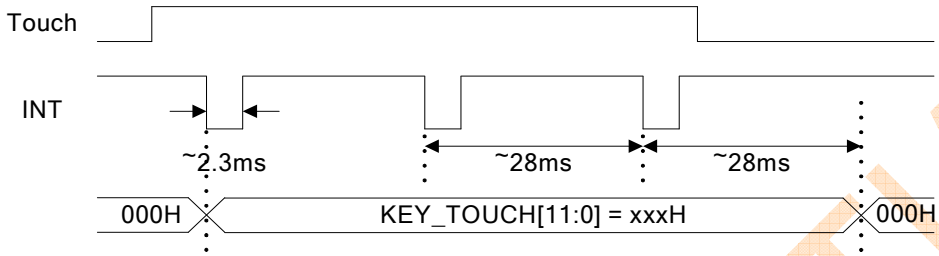
Index	Default	R/W	Bit	Name	Description
0E	**30**	R/W	7-4	Reserved"3"	must be "**3**"
			3-0	CHAN_SEL[3:0]	Select key input channel. 0000: Select sensor input SI[0] 0001: Select sensor input SI [1] | | 1010: Select sensor input SI [10] 1011: Select sensor input SI [11] 1100~1111: no define
1E	00	R	7-3	Reserved	
	00	R	2-0	SMP_CNT[10:8]	Sample counter[10:8] *
1F	00	R	7-0	SMP_CNT[7:0]	Sample counter[7:0] *

(a) After the sample channel is selected by CHAN_SEL[3:0], MCU must wait at least 28ms(@VDD=3.3V) and then read sample counter.

4.6. Interrupt

4.6.1. WT5700 ⇔ MCU interface timing

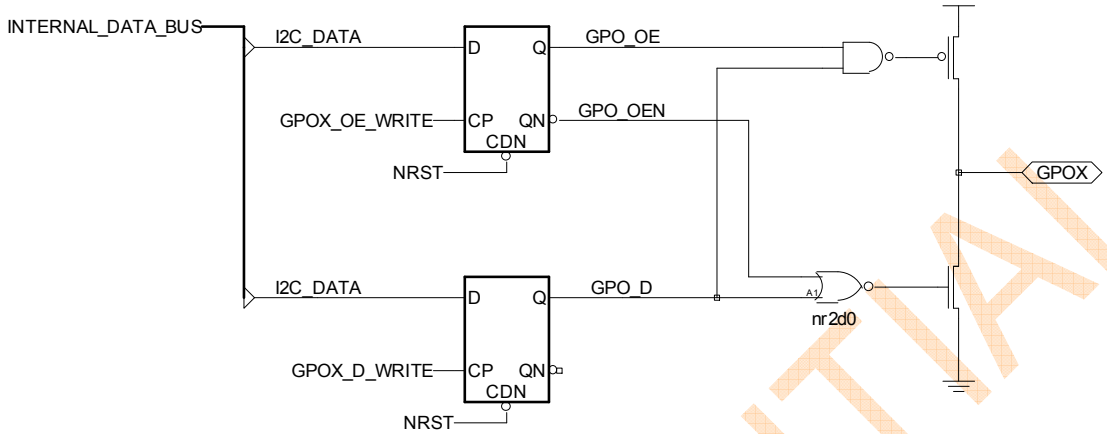
When any key pads are touched, the INT pin generates periodic pulse which period ~=28ms(@VDD=3.3V). ACT_INT_LVL register((index:00H,bit3)) controls to program H/L active level of INT pin



After “INT” is active, MCU must read KEY_TOUCH among 28ms. Otherwise, MCU maybe read KEY_TOUCH[11:0]=000H

4.7. Output expander shared with OUT[5:0] pins

The GPO[0] ~ GPO[5] are the general purpose output shared with KEY detector output pads. When GPO_OE is enable, it is a general purpose output port and it could source /sink 4mA.



Index	Default	R/W	Bit	Name	Description
04	00	R/W	7-6	Reserved	
			5-0	GPO_OE[5:0]	GPO output enable 1: GPO_D[5:0] output 0: detector OUT[5:0] output
05	00	W	7-6	Reserved	
			5-0	GPO_D[5:0]	Write: GPO output data

5. Electrical Characteristics

5.1. Absolute Maximum Ratings

Parameter	Min.	Max.	Units
DC Supply Voltage (VDD)	-0.3	5.5	V
Storage temperature	-25	125	°C
Operating temperature	-10	85	°C

***Note: Stresses above those listed may cause permanent damage to the devices**

5.2. Power Supply

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
I_{VDD5v}	Normal operation current at 5V operating	No load on output		315		uA
I_{VDD33v}	Normal operation current at 3.3V operating	No load on output		150		uA
I_{SLOW5v}	Slow down mode current at 5V operating	No load on output		75		uA
$I_{SLOW33v}$	Slow down mode current at 3.3V operating	No load on output		35		uA
$I_{SLEEP5v}$	Sleep mode current at 5V operating	No load on output			1	uA
$I_{SLEEP33v}$	Sleep mode current at 3.3V operating	No load on output			1	uA

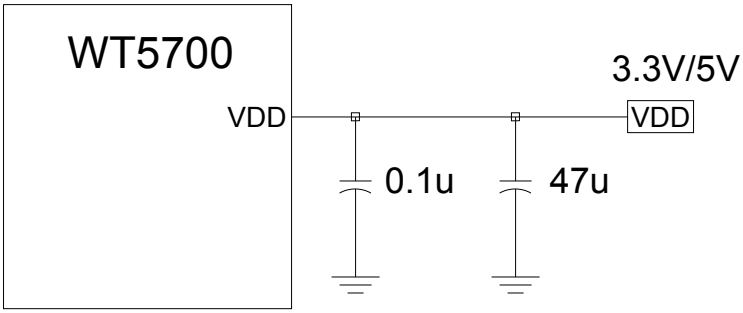
5.3. Digital I/O

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
V_{IH}	Input high Voltage		$0.7V_{DD}$		V_{DD}+0.3	V
V_{IL}	Input low voltage		-0.3		0.2VDD	V
V_{OH}	Output high voltage (Note 1)	I_{OH} = 4mA at VDD= 3.3V	2.4			V
V_{OH}	Output high voltage (Note 1)	I_{OH} = 4mA at VDD= 5V	4			V
V_{OL}	Output low voltage (Note 2)	I_{OL} = 4mA			0.4	V
V_{OL}	Output low voltage (Note 3)	I_{OL} = 8mA			0.4	V
I_{OZ}	Tri-state leakage current	V_O = 0 or 3.3V		±0.01	±1	μA
R_{PU1}	Pull up resistor (Note 4)	VDD=5V		25		KΩ
R_{PU2}	Pull up resistor (Note 5)	VDD=5V		10		MΩ

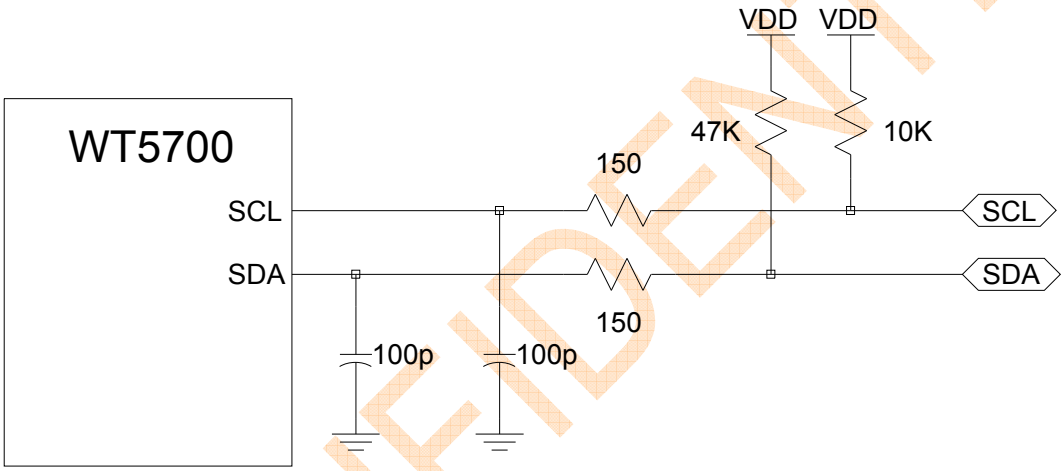
Note 1: Including all output PAD.
Note 2: Including INT, SDA and PWMO[1:0] output PAD
Note 3: Including OUT[11:0] output PAD
Note 4: Including SCL and SDA
Note 5: Including TEST, MTM, SLOW_MODE_N, WIN_CTL, SENSE[2:0], PWMO_EN and PWMO_SLT

6. Typical Application Circuit

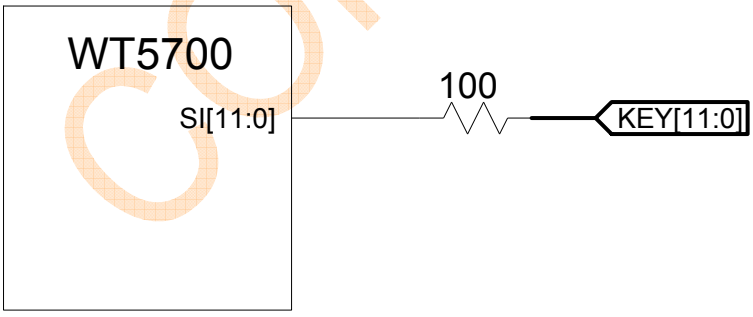
6.1. VDD Pin



6.2. I2C Interface Protection

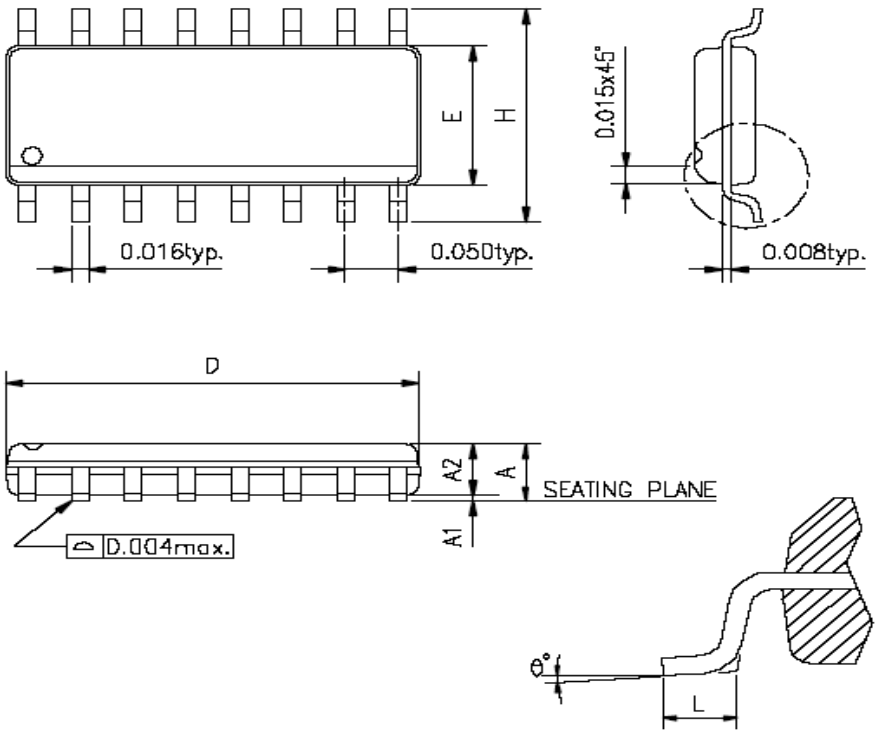


6.3. SI[11:0] Input Protection



7. Package Dimension

7.1. 16pin SOP

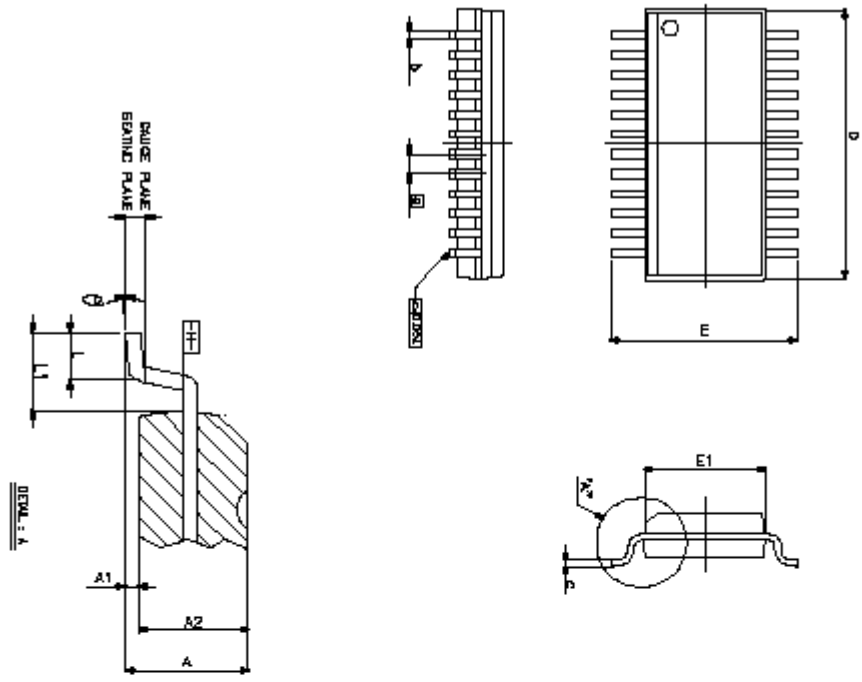


SYMBOLS	MIN.	MAX.
A	0.053	0.069
A1	0.004	0.010
D	0.386	0.394
E	0.150	0.157
H	0.228	0.244
L	0.016	0.050
θ°	0	8

UNIT : INCH

NOTES:
1. JEDEC OUTLINE : MS-012 AC
2. DIMENSIONS "D" DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS MOLD FLASH, PROTRUSIONS AND GATE BURRS SHALL NOT EXCEED .15mm (.006in) PER SIDE.
3. DIMENSIONS "E" DOES NOT INCLUDE INTER-LEAD FLASH, OR PROTRUSIONS. INTER-LEAD FLASH AND PROTRUSIONS SHALL NOT EXCEED .25mm (.010in) PER SIDE.

7.2. 24pin SSOP



SYMBOLS	MIN.	NOM.	MAX.
A	—	0.084	0.070
A1	0.004	—	—
A2	—	—	0.059
b	0.008	—	0.012
c	0.006	—	0.010
D	0.335	0.341	0.346
E	0.228	0.236	0.244
E1	0.150	0.154	0.157
e	0.020	0.025	0.030
L	0.016	0.025	—
L1	—	0.041	—
θ°	0°	—	8°

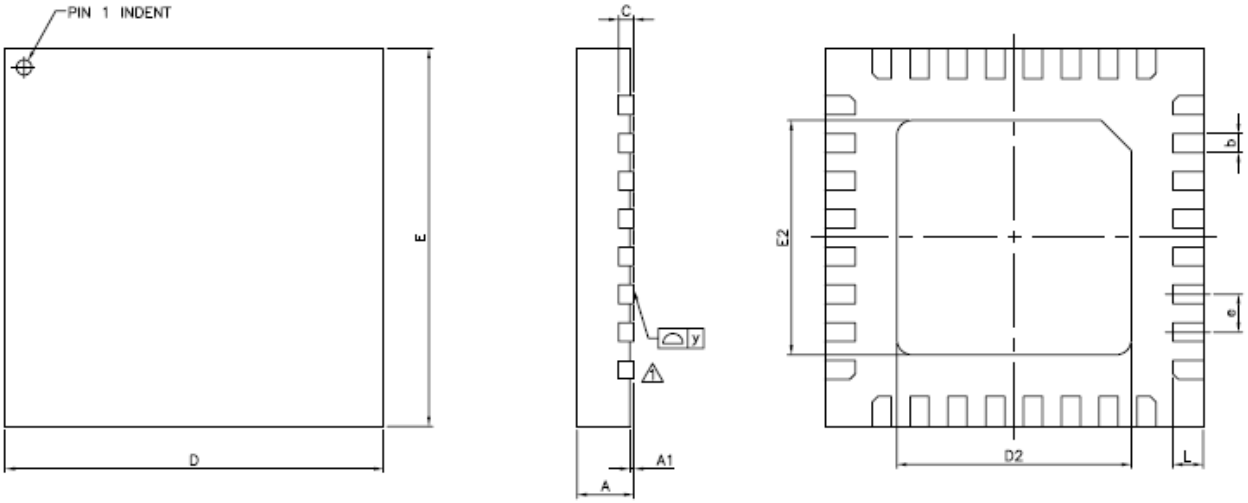
UNIT : INCH

NOTES:

1.DIMENSION D DOES NOT INCLUDE MOLD PROTRUSIONS OR GATE BURRS. MOLD PROTRUSIONS AND GATE BURRS SHALL NOT EXCEED 0.006" PER SIDE. DIMENSION E1 DOES NOT INCLUDE INTERLEAD MOLD PROTRUSIONS. INTERLEAD MOLD PROTRUSIONS SHALL NOT EXCEED 0.010" PER SIDE.

2.DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION/INTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.004" TOTAL IN EXCESS OF b DIMENSION AT MAXIMUM MATERIAL CONDITION. DAMBAR INTRUSION SHALL NOT REDUCE DIMENSION b BY MORE THAN 0.002" AT LEAST.

7.3. 32pin QFN

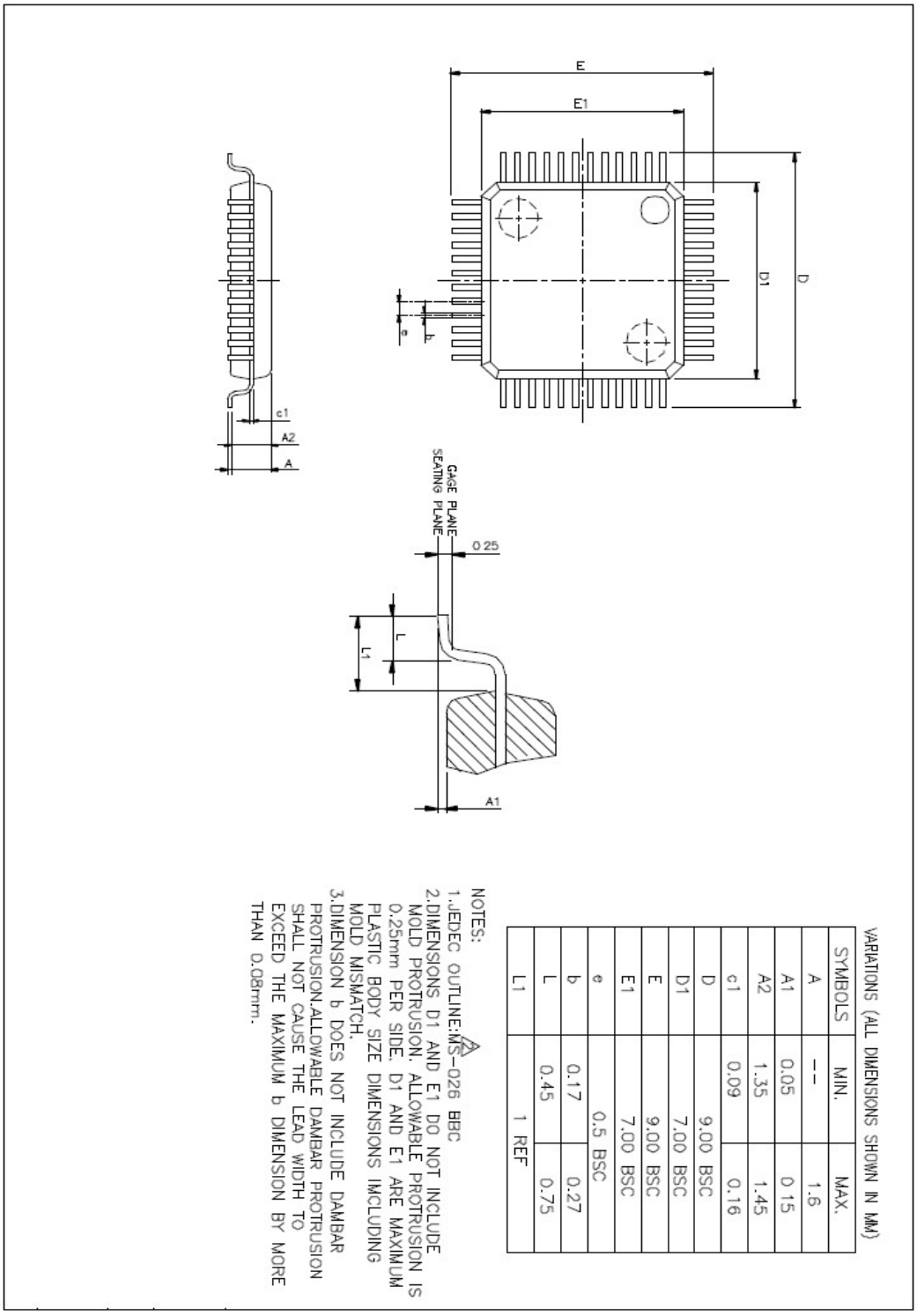


SYMBOLS	DIMENSIONS IN MILLIMETERS		
	MIN	NOM	MAX
A	0.70	0.75	0.80
A1	0.00	0.02	0.05
b	0.18	0.25	0.30
C	——	0.20 REF.	——
D	4.90	5.00	5.10
D2	3.05	3.10	3.15
E	4.90	5.00	5.10
E2	3.05	3.10	3.15
e	——	0.50	——
L	0.35	0.40	0.45
y	0.00	——	0.075

NOTE:

1.THE TERMINAL #1 IDENTIFIER IS A LASER MARKED FEATURE

7.4. 48pin LQFP



VARIATIONS (ALL DIMENSIONS SHOWN IN MM)

SYMBOLS	MIN.	MAX.
A	--	1.6
A1	0.05	0.15
A2	1.35	1.45
c1	0.09	0.16
D	9.00 BSC	
D1	7.00 BSC	
E	9.00 BSC	
E1	7.00 BSC	
e	0.5 BSC	
b	0.17	0.27
L	0.45	0.75
L1	1 REF	

NOTES:
1.JEDEC OUTLINE:MS-026 BBC
2.DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.25mm PER SIDE. D1 AND E1 ARE MAXIMUM PLASTIC BODY SIZE DIMENSIONS INCLUDING MOLD MISMATCH.
3.DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION.ALLOWABLE DAMBAR PROTRUSION SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED THE MAXIMUM b DIMENSION BY MORE THAN 0.08mm.